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| 10/038,431 | 12/31/2001 | Sushma Shrikant Trivedi | 04860.P2687 | 7868 |

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| EXAMINER | |
|---|---|
| LI, AIMEE J | |
| ART UNIT | PAPER NUMBER |
| 2183 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/12/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/038,431 | TRIVEDI ET AL. | |
| | Examiner | Art Unit | |
| | Aimee J. Li | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9-18,20-32 and 34-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-18, 20-32, and 34-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-7, 9-18, 20-32, and 34-41 have been examined. Claims 1, 12, and 26 have been amended as per Applicant's request.

### *Papers Submitted*

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as filed 30 October 2006.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier).

5. Regarding claims 1, 12, 23, and 26, taking claim 1 as exemplary, Chehrazi has taught a method for execution by a microprocessor in response to receiving a single instruction (Chehrazi Col.20 lines 42-52), the method comprising:

a. Receiving a first vector of numbers and a second vector of numbers (Chehrazi 310 of Fig.20B, Col.20 line 62 – Col.21 line 1);

b. Selecting a first plurality of numbers from a first vector (Chehrazi 310 of Fig.20B, Col.20 line 62 – Col.21 line 1) and a second plurality of numbers from the second

vector (Chehrazi 312 of Fig.20B, Col.20 line 62 – Col.21 line 1) according to a configuration specified by the instruction (Chehrazi 560 of Fig 20A, Col.20 line 42 – Col.21 line 13), and

c. Generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers (Chehrazi Col.21 lines 6-12),

d. Wherein the sum of third plurality of numbers are saved in an entry in a register file (Chehrazi Col.20 lines 47-58),

e. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (Chehrazi Col.20 lines 42-52, 61-62).

6. Chehrazi has not explicitly taught wherein the third plurality of numbers themselves are saved in an entry in a register file. However, Mennemeier has taught storing a third plurality of numbers, specifically a vector of absolute differences, in a instruction specified register (Mennemeier, Col.7 line 64 – Col.8 line 23) so that the absolute differences can be used in other operations that require the distance assessment that the results represent (Mennemeier, Col.8 line 21-23). One of ordinary skill in the art would have recognized that it is desirable to retain results that will be used by future instructions so that the results don't need to be recalculated. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chehrazi to store the absolute differences, rather than the sum of the absolute differences, in an instruction specified register so that the values could be reused by other operations that require the data, thus improving throughput by avoiding the recalculation of the data.

7. Claims 12, 23, and 26 are nearly identical to claim 1. However, Chehrazi has taught the differences. Claim 12 differs in the claim being comprised within a machine-readable media (Chehrazi Col.20 lines 42-46), while claims 23 and 26 differs in the claims being comprised within an execution unit (Chehrazi Col.7 lines 20-40). Also, claim 23 claims wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54). Besides these differences, the claims encompass the same scope as claim 1. Thus, claims 12, 23 and 26 are rejected for the same reasons as claim 1.

8. Regarding claims 2, 13, 24 and 27, taking claim 2 as exemplary, Chehrazi has taught a method as in claim 1, wherein an absolute difference between a first number and a second number is computed using a method comprising:

a. Producing a first intermediate number by subtracting the second number from the first number (Chehrazi Col.21 lines 1-8),

b. Producing a second intermediate number by subtracting the first number from the second number (Chehrazi Col.21 lines 1-8),

c. Selecting a positive number from the first intermediate number and the second intermediate number as the absolute difference between the first number and the second number (Chehrazi Col.21 lines 8-12),

d. Wherein the microprocessor is a media processor (Chehrazi 108 of Fig.1, Col.3 lines 6-7) disposed on an integrated circuit with a memory controller (Chehrazi 100 of Fig.1, Col.5 lines 46-54).

9. Claims 13, 24 and 27 are nearly identical to claim 2. Claim 13 lacks the recitation of a media processor disposed on an integrated circuit with a memory controller, and claims 13, 24

and 27 differ in their parent claims, but encompass the same scope as claim 2. Thus, claims 13, 24 and 27 are rejected for the same reasons as claim 2.

10. Regarding claims 3, 14 and 28, taking claim 3 as exemplary, Chehrazi has taught a method as in claim 2, wherein the first intermediate number and the second intermediate number are produced in parallel (Chehrazi Col.21 lines 1-8), and wherein the third plurality of numbers are generated substantially simultaneously (Chehrazi Col.21 lines 8-12).

11. Claims 14 and 28 are nearly identical to claim 3, both differing in their lack of having the third plurality of numbers being generated substantially simultaneously, as well as differing in their parent claims, but both encompass the same scope as claim 3. Thus, Claims 14 and 28 are rejected for the same reasons as claim 3.

12. Regarding claims 5, 16 and 30, taking claim 5 as exemplary, Chehrazi has taught a method as in claim 1, wherein the first plurality of numbers are received from a first entry in the register file (Chehrazi Col.20 lines 47-58).

13. Claims 16 and 30 are nearly identical to claim 5, differing in their parent claims, but encompassing the same scope as claim 5. Thus, claims 16 and 30 are rejected for the same reasons as claim 5.

14. Regarding claims 6, 17 and 31, taking claim 6 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies a way to partition a string of bits in the first entry into a first plurality of numbers (Chehrazi Col.20 lines 61-65). Here, the SABD instruction specifies a register in the register file, which corresponds to the plurality of numbers, and specifies that the data in the register be interpreted to be 16 separate 8-bit numbers.

15. Claims 17 and 31 are nearly identical to claim 6, differing in their parent claims, but encompassing the same scope as claim 6. Thus, claims 17 and 31 are rejected for the same reasons as claim 6.

16. Regarding claims 7, 18 and 32, taking claim 7 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies an index of the entry in the first register file (Chehrazi 560c and 560d of Fig.20a, Col.20 lines 47-58).

17. Claims 18 and 32 are nearly identical to claim 7, differing in their parent claims, but encompassing the same scope as claim 7. Thus, claims 18 and 32 are rejected for the same reasons as claim 7.

18. Regarding claims 9, 20 and 34, taking claim 9 as exemplary, Chehrazi in view of Mennemeier has taught a method as in claim 1, wherein the single instruction specifies an index of the entry in a the register file (Mennemeier, Col.7 line 64 – Col.8 line 23, as well as above paragraph 39).

19. Claims 20 and 34 are nearly identical to claim 9, differing in their parent claims, but encompassing the same scope as claim 9. Thus, claims 20 and 34 are rejected for the same reasons as claim 9.

20. Regarding claims 10, 21 and 35, taking claim 10 as exemplary, Chehrazi has taught a method as in claim 1, wherein a type of each of the first and second pluralities of numbers is one of:

a. Unsigned integer (Chehrazi Col.20 lines 54-55),

b. Signed integer (Chehrazi Col.20 lines 54-55),

c. Floating-point number.

21. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 10.

22. Claims 21 and 35 are nearly identical to claim 10, differing in their parent claims, but encompassing the same scope as claim 10. Thus, claims 21 and 35 are rejected for the same reasons as claim 10.

23. Regarding claim 11, 22 and 36, taking claim 11 as exemplary, Chehrazi has taught a method as in claim 1, wherein a size of each of the first and second pluralities of numbers is one of:

a. 8 bits (Chehrazi Col.20 lines 61-65),

b. 16 bits,

c. 32 bits.

24. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 11.

25. Claims 22 and 36 are nearly identical to claim 11, differing in their parent claims, but encompassing the same scope as claim 11. Thus, claims 22 and 36 are rejected for the same reasons as claim 11.

26. Regarding claim 25, Chehrazi has taught a processing system comprising an execution unit as in claim 23 (Chehrazi Fig.1).

27. Regardin claim 37, Chehrazi has taught wherein a type of each of the first and second pluralities of numbers is floating point number (Chehrazi column 1, lines 19-21 and column 9, lines 37-41).

28. Regarding claim 38, Chehrazi has taught wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54).

29. Regarding claim 40, Chehrazi has taught wherein the memory controller is usable to access memory not disposed on the integrated circuit (Chehrazi Col. 5 lines 36-60 and Figure 1). As can be seen in Chehrazi's Figure 1, the ROM and RAM memories and data storage device are separate from the processor.

30. Regarding claim 41, Chehrazi has taught wherein the memory controller is usable by a host central processing unit not disposed on the integrated circuit to access the memory (Chehrazi Col. 5 lines 36-60 and Figure 1). As can be seen in Chehrazi's Figure 1, the ROM and RAM memories and data storage device are separate from the processor.

31. Claims 4, 15, 29, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier) as applied to claims 1, 2, 12, 26, and 27 above, and further in view of Diefendorff et al., EPO 0 485 776 A2 (herein referred to as Diefendorff).

32. Regarding claims 4, 15, 29, and 39, taking claim 4 as exemplary, Chehrazi has taught taking an absolute difference between a first number and a second number (Chehrazi Col.21 lines 6-12). Chehrazi has not taught:

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number,

b. Saturating the difference between the first number and the second number if an overflow occurs.

33. Diefendorff has taught

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5),

b. Saturating the difference between the first number and the second number if an overflow occurs (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5).

34. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Diefendorff, that overflow testing and saturation arithmetic improves the handling of overflow conditions during shading or image processing, thereby improving the quality of the image and accelerating the performance of the microprocessor during shading and image processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the overflow testing and saturation arithmetic of Diefendorff in the device of Chehrazi to improve image quality and accelerate the performance of a microprocessor during shading and image processing.

***Response to Arguments***

35. Applicant's arguments filed 16 May 2006 have been fully considered but they are not persuasive.

36. Applicant argues in essence on pages 13 and 14-15

> ...Chehrazi does not teach or suggest a combination with Mennemeir and Diefendorff, and Mennemeir does not teach or suggest a combination with Chehrazi and Diefendorff, and Diefendorff does not teach or suggest a combination with Chehrazi and Mennemeir...It would be impermissible hindsight based on Applicants own disclosure to combine Chehrazi and Mennemeir.

37. This has not been found persuasive. Applicant's current arguments alleging impermissible hindsight due to nonanalogous art attempts to suggest that Chehrazi and Mennemeir are for two different fields of endeavor. Applicants attempt to show this by stating that "Chehrazi teaches pipelining for a media processor. Mennemeir, in contrast, teaches sorting signed packed numbers. Diefendorff, in contrast to Mennemeier and Chehrazi, teaches executing of a graphics pixel packing instruction (Abstract)." However, Chehrazi, Mennemeir, and Diefendorff are all in the field of multimedia pipelined processors (Chehrazi column 1, lines 22-40; Mennemeir column 1, lines 22-25 and 56-59; and Diefendorff column 1, lines 20-25). Chehrazi focuses on the data path of an instruction, e.g. what elements are needed to execute an instruction; Mennemeir focuses on the data instructions uses, e.g. packed data and how it must be handled by instructions; and Diefendorff focuses specific instructions used during high speed graphics rendering. Also, Chehrazi has taught that packed data is present in his system in column 3, lines 15-20 by stating that the operand registers are 128-bits and the multiply operation performs one 128x128 multiply operation, e.g. one multiply operation on a single piece of data that is 128-bits wide in the operand registers; four 32x32 multiply operations, e.g. four multiply operations on the four pieces of data that are 32-bits wide each in the operand registers; eight 16x16 multiply operations, e.g. eight multiply operations on the eight pieces of data that are

16-bits wide each in the operand registers; or sixteen 8x8 multiply operations; e.g. sixteen multiply operations on the sixteen pieces of data that are 8-bits wide each in the operand registers. As Mennemeir has taught in column 1, lines 28-45, packed data is "a number of data elements...grouped together into a common bit string having a specified width", which are the data elements found in Chehrazi's operand registers. Simply because Chehrazi has not called the data in the operand registers "packed data" does not mean that Chehrazi does not handle packed data. As stated previously, Chehrazi was focused on the data path an instruction follows, but does not go into the details of how to handle the packed data in the instructions or the instructions specifically needed to render the graphics on a display screen. Mennemeir has more details on how the data is handled and was combined to teach the details on packed data handling missing in Chehrazi, and Diefendorff has the details on the instructions needed to correctly render graphics on a display screen . In response to applicant's argument that Mennemeir, Chehrazi, and Diefendorff are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the

applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

38. Applicants argue in essence on pages 13 and 14

> ...if Chehrazi and Mennemeir were combined, such a combination would selecting a first plurality of numbers from the first vector and a second plurality of numbers from the second vector according to a configuration specified by the instruction...
>
> ...
>
> ...neither Chehrazi, Mennemeir, nor a combination thereof, discloses a selector circuit configured to select a first plurality of numbers from the first vector and a second plurality of numbers from the second vector...

39. This has not been found persuasive. Chehrazi has taught that the SABD instruction uses the data in the registers to find the absolute difference. Specifically, Chehrazi selects the operands from the first vector register as a first plurality of numbers and the operands from the second vector register as a second plurality of numbers according to the source registers specified by the instruction. Also, Chehrazi has taught that the SABD instruction actually performs two subtraction operations: Vs-Vt and Vt-Vs, and selects via a multiplexer the positive values from the results from each of the resulting two vectors (Chehrazi column 9, lines 6-26; column 20, line 42 to column 21, line 12; Figure 4; Figure 20A; and Figure 20B). Thus, Chehrazi receives two vectors of numbers, e.g. the two source vectors or the two result vectors from the two separate subtraction operations; selects numbers from each vector according to a configuration specified by the instruction, e.g. selects the associated numbers from each of the

source vectors specified by the instruction for subtraction or all the positive numbers in the two subtraction result vectors since the instruction specifies that the absolute difference is wanted; and generates a vector of the absolute difference. Applicants' arguments seem to suggest that the claim language means to limit the selection to only portions of the vectors, however, that is not clear by the claim language, and, as stated above, only portions of the two subtraction result vectors are chosen, since only the positive results are selected by the multiplexer. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., selecting a plurality of numbers is only a portion of the data available in the register) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

## *Conclusion*

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
07 January 2007

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